Multiplexed Inputs/Outputs Provide Improved Bit Density

Four Modes of Operation:
- Hold (Store) Shift Left
- Shift Right Load Data

Operates with Outputs Enabled or at High Z

3-State Outputs Drive Bus Lines Directly

Can Be Cascaded for N-Bit Word Lengths

Typical Power Dissipation ... 175 mW

Exceptionally Stable Shift (Clock)
Frequency ... 25 MHz

Applications:
- Stacked or Push-Down Registers,
- Buffer Storage, and
- Accumulator Registers

SN54LS299 and SN74LS299 Are Similar
But Have Direct Overriding Clear

These Low-Power Schottky eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table. Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. The clear function is synchronous, and a low level at the clear input clears the register on the next low-to-high transition of the clock.

**FUNCTION TABLE**

<table>
<thead>
<tr>
<th>MODE</th>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CLR</td>
<td>FUNCTION</td>
</tr>
<tr>
<td></td>
<td>S1</td>
<td>S0</td>
</tr>
<tr>
<td>Clear</td>
<td>L</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>L</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>L</td>
<td>M</td>
</tr>
<tr>
<td>Hold</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td></td>
<td>H</td>
<td>X</td>
</tr>
<tr>
<td>Shift Right</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td></td>
<td>H</td>
<td>M</td>
</tr>
<tr>
<td>Shift Left</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td></td>
<td>H</td>
<td>M</td>
</tr>
<tr>
<td>Load</td>
<td>H</td>
<td>M</td>
</tr>
<tr>
<td></td>
<td>H</td>
<td>M</td>
</tr>
</tbody>
</table>

**Inputs/Outputs**

- Serial: A/0A, B/0B, C/0C, D/0D, E/0E, F/0F, G/0G, H/0H
- Outputs: A/0A, B/0B, C/0C, D/0D, E/0E, F/0F, G/0G, H/0H

*When one or both output controls are high the eight input/output terminals are disabled in the high-impedance state; however, sequential operation or clearing of the register is not affected.

a...h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip flops while the flip-flop outputs are isolated from the input/output terminals.
SN54LS323, SN74LS323
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

logic symbol†

†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, N, and W packages.

logic diagram (positive logic)

Pin numbers shown are for DW, J, N, and W packages.
schematics of inputs and outputs, absolute maximum ratings, recommended operating conditions, and electrical characteristics

Same as SN54LS299 and SN74LS299, except \( t_{\text{au}} \) (Clear inactive) does not apply.

switching characteristics, \( V_{\text{CC}} = 5 \, \text{V}, \, T_{\text{A}} = 25^\circ \text{C} \)

<table>
<thead>
<tr>
<th>PARAMETER(^1)</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>f(_{\text{max}})</td>
<td>CLK</td>
<td>( Q_A ) or ( Q_H )</td>
<td>( C_L = 15 , \text{pF}, , R_L = 2 , \text{k})</td>
<td>22</td>
<td>26</td>
<td>33</td>
<td>( \text{ns} )</td>
</tr>
<tr>
<td>t(_{\text{PLH}})</td>
<td>CLK</td>
<td>( Q_A ) thru ( Q_{H1} )</td>
<td>( C_L = 45 , \text{pF}, , R_L = 665 , \Omega )</td>
<td>17</td>
<td>25</td>
<td>25</td>
<td>( \text{ns} )</td>
</tr>
<tr>
<td>t(_{\text{PHL}})</td>
<td>( G_1, G_2 )</td>
<td>( Q_A ) thru ( Q_H )</td>
<td>( C_L = 5 , \text{pF}, , R_L = 665 , \Omega )</td>
<td>14</td>
<td>21</td>
<td>20</td>
<td>( \text{ns} )</td>
</tr>
<tr>
<td>t(_{\text{PHZ}})</td>
<td>( G_1, G_2 )</td>
<td>( Q_A ) thru ( Q_{H1} )</td>
<td>( C_L = 15 , \text{pF}, , R_L = 2 , \text{k})</td>
<td>26</td>
<td>36</td>
<td>33</td>
<td>( \text{ns} )</td>
</tr>
</tbody>
</table>

\( f_{\text{max}} \) = maximum clock frequency

\( t_{\text{PLH}} \) = Propagation delay time, low-to-high-level output

\( t_{\text{PHL}} \) = Propagation delay time, high-to-low-level output

\( t_{\text{PHZ}} \) = Output enable time to high level

\( t_{\text{PLZ}} \) = Output enable time to low level

\( t_{\text{PHZ}} \) = Output disable time from high level

\( t_{\text{PLZ}} \) = Output disable time from low level

\( \text{NOTE 1: For testing } f_{\text{max}} \text{, all outputs are loaded simultaneously, each with } C_L \text{ and } R_L \text{ as specified for the propagation times.} \)

\( \text{Load circuits and voltage waveforms are shown in Section 1.} \)
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